In the Claims:

1-2. (Cancelled)

3. (Currently Amended) A method for forming a plurality of three-dimensional structures on a substrate, the method comprising:

providing a wafer with bumps distributed on a surface of the wafer, said bumps on said wafer comprising compliant elements; [[and]]

forming a resist over the surface of the wafer including the bumps by coating the surface of the wafer with an electrophoretic resist by dipping the surface of the wafer into the resist and by applying an electrical voltage between the wafer and the electrophoretic ~~resist.~~ resist; and

patterning said resist and forming a conductor overlying one of said bumps to provide a three dimensional structure having a terminal supported by one of said compliant bumps.

4. (Previously Presented) The method of claim 13 and further comprising:

removing the surface of the wafer with the bumps from the electrophoretic resist; and

patterning the electrophoretic resist after removing the surface of the wafer from the electrophoretic resist.

5. (Cancelled)

6. (Previously Presented) The method of claim 13 wherein forming a plurality of conductors comprises:

forming a copper layer over portions of the seed layer not covered by the electrophoretic resist;

forming a nickel layer over the copper layer; and

forming a gold layer over the nickel layer.

7. (Previously Presented) A method for forming a plurality of three-dimensional structures on a semiconductor wafer, the method comprising:

providing a wafer with bumps distributed on a surface of the wafer;

forming a resist over the surface of the wafer including the bumps by coating the surface of the wafer with an electrophoretic resist by dipping the surface of the wafer into the resist and by applying an electrical voltage between the wafer and the electrophoretic resist; and

patterning the resist to expose the surface of the wafer and forming a plurality of conductors over the exposed surface of the wafer, said plurality of conductors comprising a reroute layer electrically coupling a contact pad formed on the semiconductor wafer to a terminal on the surface of the wafer.

8. (Cancelled)

9. (Previously Presented) The method of claim 13 and further comprising causing the wafer surface with the bumps to be moved relative to the electrophoretic resist while the wafer surface is in the electrophoretic resist.

10. (Previously Presented) The method of claim 9 wherein the wafer surface is rotated while the wafer surface is in the electrophoretic resist.

11. (Previously Presented) The method of claim 9 wherein the electrophoretic resist is stirred while the wafer surface is in the electrophoretic resist.

12. (Previously Presented) The method of claim 4 and further comprising heating the substrate after removing the wafer surface from the electrophoretic resist.

13. (Previously Presented) A method for forming a plurality of three-dimensional structures on a substrate, the method comprising:

providing a wafer with bumps distributed on a surface of the wafer;

forming a resist over the surface of the wafer including the bumps by coating the surface of the wafer with an electrophoretic resist by dipping the surface of the wafer into the resist and by applying an electrical voltage between the wafer and the electrophoretic resist;

patterning the resist to expose an underlying surface; and

forming a plurality of conductors over the exposed said underlying surface wherein the plurality of conductors electrically connect bonding pads on the wafer to terminals located on the bumps.

14-15. (Cancelled)

16. (Original) The method of claim 13 wherein the surface of the wafer is dipped into the electrophoretic resist in a horizontal arrangement of the wafer.

17. (Original) The method of claim 16 wherein a rear side of the wafer is protected from wetting during the process of dipping into the electrophoretic resist.

18. (Original) The method of claim 13 wherein the wafer is caused to rotate during the coating operation.

19. (Original) The method of claim 13 wherein a flow is produced at least below the wafer in the electrophoretic resist during the coating operation.

20. (Original) The method of claim 19 wherein the electrophoretic resist is caused to rotate in a region of the surface of the wafer.

21. (Original) The method of claim 20 wherein the rotation of the electrophoretic resist is produced by a stirrer.

22. (Original) The method of claim 13 wherein the wafer is removed in a horizontal position after the process of coating with the electrophoretic resist and the coating is baked thermally.

23. (Previously Presented) The method of claim 3 further comprising:

removing the surface of the wafer with the bumps from the electrophoretic resist; and

patterning the electrophoretic resist after removing the surface of the wafer from the electrophoretic resist.

24. (Previously Presented) The method of claim 23 and further comprising heating the substrate after removing the wafer surface form the electrophoretic resist.

25. (Currently Amended) The method of claim 23 wherein the ~~plurality of conductors~~ conductor electrically ~~connect~~ connects a bonding [[pads]] pad on the wafer to ~~terminals~~ said terminal located on the bumps.

26. (Previously Presented) The method of claim 3 and further comprising:

patterning the resist to expose a seed layer over the surface of the wafer; and

forming a plurality of conductors over the exposed seed layer.

27. (Previously Presented) The method of claim 26 wherein forming a plurality of conductors comprises:

forming a copper layer over portions of the seed layer not covered by the electrophoretic resist;

forming a nickel layer over the copper layer; and

forming a gold layer over the nickel layer.

28. (Previously Presented) The method of claim 7 wherein said step of exposing the surface of the wafer exposes a seed layer.

29. (Previously Presented) The method of claim 13 wherein said step of exposing an underlying surface exposes a seed layer.